WHAT IS CLAIMED IS:

1. An integrated DRAM semiconductor memory, comprising:

local data lines segmented in a column direction and having a CSL switch, which connects the local data lines in response to a column select signal fed via a CSL line running in a row direction to primary sense amplifiers, at least during one of a read or write cycle, for transferring and accepting spread data signals to and from bit lines of a respective segment; and

LDQ switches arranged at interfaces between adjacent segments of the local data lines for their connection to the local data lines of adjacent segments, which LDQ switches, depending on a control signal fed separately to each of said LDQ switches, are closed during a precharge phase, which takes place before each read cycle, of at least two adjacent LDQ segments.

2. The DRAM semiconductor memory as in claim 1, wherein the LDQ switches that are closed during a precharge phase are otherwise open.

3. The DRAM semiconductor memory as in claim 1, wherein the CSL switch connects the local data lines in response to a column select signal fed via a CSL line during a read and write cycle.

4. The DRAM semiconductor memory as in claim 1, wherein each LDQ switch is assigned an AND element in order to logically combine the precharge phase condition of the at least two adjacent LDQ segments and to generate therefrom the control signal for the respective LDQ switch.

5. The DRAM semiconductor memory as in claim 3, wherein local data lines of a segment are connected via an MDQ switch to a main data line, which runs in the row direction and is common to local data lines of a segment, and to a secondary sense amplifier for accepting/transferring spread data signals in a write/read cycle.

6. The DRAM semiconductor memory as in claim 1, wherein cell arrays of the semiconductor memory are subdivided in the row direction into individual cell blocks between which run, in the column direction, a sense amplifier strip with the primary sense amplifiers and the associated CSL switches, the local data lines, the MDQ switches and the LDQ switches likewise being arranged in said sense amplifier strip and the secondary sense amplifiers and the AND elements which generate the control signal being arranged in a chip belt of the integrated semiconductor memory.

7. The DRAM semiconductor memory as in claim 3, wherein the write and read data are complementary data, and wherein the local data lines and the main data lines are arranged as complementary data lines.

8. The DRAM semiconductor memory as in claim 7, wherein, the CSL switches, the MDQ switches and the LDQ switches are arranged for the complementary local and main data lines as FET transistor pairs with common gate driving.

9. A method for operating an integrated DRAM semiconductor memory, comprising:

providing local data lines segmented in a column direction and main data lines running in a row direction, having main data lines being common to local data lines of an LDQ segment and local data lines being connected by a common select line (CSL) switch in response to a column select signal fed to the latter, during at least one of a read or write cycle, to a primary sense amplifier for reading or writing of spread data; and

connecting the local data lines of at least two adjacent LDQ segments to one another during a precharge phase before each read cycle, which is activated by an activation of the CSL switch by means of the column select signal.

10. The method of claim 9, further comprising assigning an AND element to an LDQ switch in order to logically combine the precharge phase condition of the at least two adjacent LDQ segments and to generate therefrom the control signal for the respective LDQ switch.

11. The method of claim 9, further comprising connecting local data lines of a segment via an MDQ switch to a main data line, which runs in the row direction and is common to local data lines of a segment, and to a secondary sense amplifier for accepting/transferring spread data signals in a write or read cycle.

12. The method of claim 9, further comprising subdividing cell arrays of the semiconductor memory in the row direction into individual cell blocks between which run, in the column direction, in each case a sense amplifier strip with the primary sense amplifiers and associated CSL switches, arranging local data lines, MDQ switches and LDQ switches in said

sense amplifier strip, and arranging secondary sense amplifiers and AND elements which generate the control signal in a chip belt of the integrated semiconductor memory.

13. The method of claim 9, wherein write and read data are complementary data, and wherein the local data lines and the main data lines are in each case arranged as complementary data lines.

14. The method of claim 13, further comprising arranging CSL switches, MDQ switches and LDQ switches in each case for the complementary local and main data lines as FET transistor pairs with common gate driving.